AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0010] with the following amended paragraph:

[0010] PDPs can use a ramp reset to obtain operational margins. When using a ramp reset to drive a PDP, wall charges are erased except the amount of wall charges that will be used for a subsequent address operation. ~~in the state that a huge amount of wall~~ Wall charges for a subsequent address operation are accumulated on the panel because of weak discharging, thereby allowing a low-voltage address operation.

Please replace paragraph [0014] with the following amended paragraph:

[0014] In Equation 1, ~~since~~ C is a capacitance of the panel.[[,]] Because the capacitance value C is constant, in order to output a ramp pulse, the current (i) applied to the panel also needs to be constant.

Please replace paragraph [0019] with the following amended paragraph:

[0019] As shown in FIG. 5, when the gate current charges the parasitic capacitance Cgs to open the FET, the current Id starts flowing. The current Id charges the parasitic capacitance Cgd and steeply rises, but it generates a voltage drop of Vr at the resistor R2 to reduce the intensity of the voltage charged to the parasitic capacitance Cgs, because the potential difference between the terminal Vs of the FET drive IC and a terminal HO for outputting a gate signal has a constant voltage Vcc (generally about 12 to 18V ~~to18V~~).

Please replace paragraph [0024] with the following amended paragraph:

[0024] In this instance, the gradients of the ramp pulse can be adjusted in the direction of arrow ① and arrow ② using resistor R1 and capacitor C1 of FIG. 5, and resistor R1 and

resistor R2 of FIG. 6. The gradients of the ramp pulse increase or decrease depending on the time constants of parts and the surrounding temperatures, because the gradients depend on the temperature characteristics of the parts.